JTAG Connector – JP1 (ALTERA)

The PMC "JTAG" signals – TDI, TDO, TRST, TMS, and TCK – are connected to 10-pin headers JP1 and JP3 on the PMC to PCI adapter. These are intended to be used for programming either ALTERA FPGA or LATTICE MACH devices on the user's PMC board.

Specifically, JP1 is used to connect a personal computer Parallel Port using ALTERA's "ByteBlasterMV" cable. The pinout of JP1 is as follows.

Signal	PMC connection	JP1 connection
TCK	PN1/JN1 – 1	1
GND	N/A	2
TDO	PN1/JN1 – 4	3
3.3V or 5V (*)	N/A	4
TMS	PN1/JN1 – 3	5
3.3V or 5V (*)	N/A	6
N/C	N/A	7
N/C	N/A	8
TDI	PN1/JN1 – 5	9
GND	N/A	10

Table 4- ALTERA JTAG header (JP1)

(*) – This is the power to the ALTERA cable. It is either 3.3V or 5V depending on JP2 jumper selection.

JP1 is also identified as "ALTERA" on the PMC to PCI adapter printed circuit board silk screened legend.

N/C – no connection made

N/A – Not applicable.

JTAG Connector – JP3 (LATTICE)

For those PMC implementations using LATTICE devices (eg. MACH family), and requiring JTAG programming through the PMC's JTAG signals, the PMC to PCI adapter provides a header – JP3 – for connection to LATTICE's ispPRO programming cable.

The pinout of JP3 is as follows.

Signal	PMC connection	JP1 connection
TCK	PN1/JN1 – 1	1
GND	N/A	2
TMS	PN1/JN1 – 3	3
GND	N/A	4
TDI	PN1/JN1 – 5	5
3.3V or 5V (*)	N/A	6
TDO	PN1/JN1 – 4	7
GND	N/A	8
TRST	PN1/JN1 – 2	9
N/C	N/A	10

Table 5- LATTICE JTAG header (JP3)

(*) – This is the power to the MACH cable. It is either 3.3V or 5V depending on JP2 jumper selection.

JP3 is also identified as "MACH" on the PMC to PCI adapter printed circuit board silk screened legend.

N/C – No connection made

N/A – Not applicable.

JTAG voltage level select jumper – JP2 (for ALTERA/MACH)

The LATTICE and ALTERA programming cables require a power supply from the target in order to power the logic in the cable. This power supplied is either 3.3V or 5V depending on the technology of the devices you are attempting to program.

The PMC to PCI adapter provides a jumper setting to select between 3.3V or 5V power to the JTAG programming headers. This jumper header is labeled "JP2" on the silk screen legend.

The 3.3V and 5V positions are established according to the following table.

JTAG cable operation	JP2 Pin #'s for jumper
3V	2-3
5V	1-2 (default)

Table 6 - JTAG voltage level select (JP2)

For user convenience, the silk screen legend on the board shows "PROG" near JP5 connector as an indication that this connector is used for configuring the JTAG cable power. Also, "5V" and "3.3V" legends indicate the jumper position for 5V and 3V operation, respectively.

JTAG Connector – JP6 (Internal Use Only)

Customers should NOT use the 10-pin connector identified as "JP6" and "INTERNAL" on the silk screen legend. This connector is used during the manufacture of the PMC to PCI adapter to effect programming of the PLD located on the board.

96-pin DIN Connections

The 96-pin DIN connector is located at the right edge of the PMC to PCI Adapter. Its purpose is to mimic the connection of the USER I/O connector (JN4/PN4) on the PMC module to the 'A' and 'C' rows of the P2 connector on a VMEbus board. This connection is fully outlined in the IEEE 1386 specification and it adheres to the following numbering strategy:

PMC I/O Pin Number	VMEbus P2 Connector Pin Number
1	c1
2	a1
3	c2
4	a2
(Continue similarly)	
63	c32
64	a32

The c1 (PMC I/O 1) connection is located near the upper edge of the PMC-to-PCI adapter board, whereas the a32 connection (PMC I/O 64) is located closest to the PCI connector.

The markings stamped on the DIN connector may be different than this because of the reverse nature of the rear I/O connector on VME backplanes. Please disregard any A and C row markings that may be stamped on the connector.

The user should fully understand the relationship between the DIN contacts and the JN2 connections before using the DIN connector. An ohmmeter is a helpful tool to check continuity between these connectors and understand the theory of operation.

Software

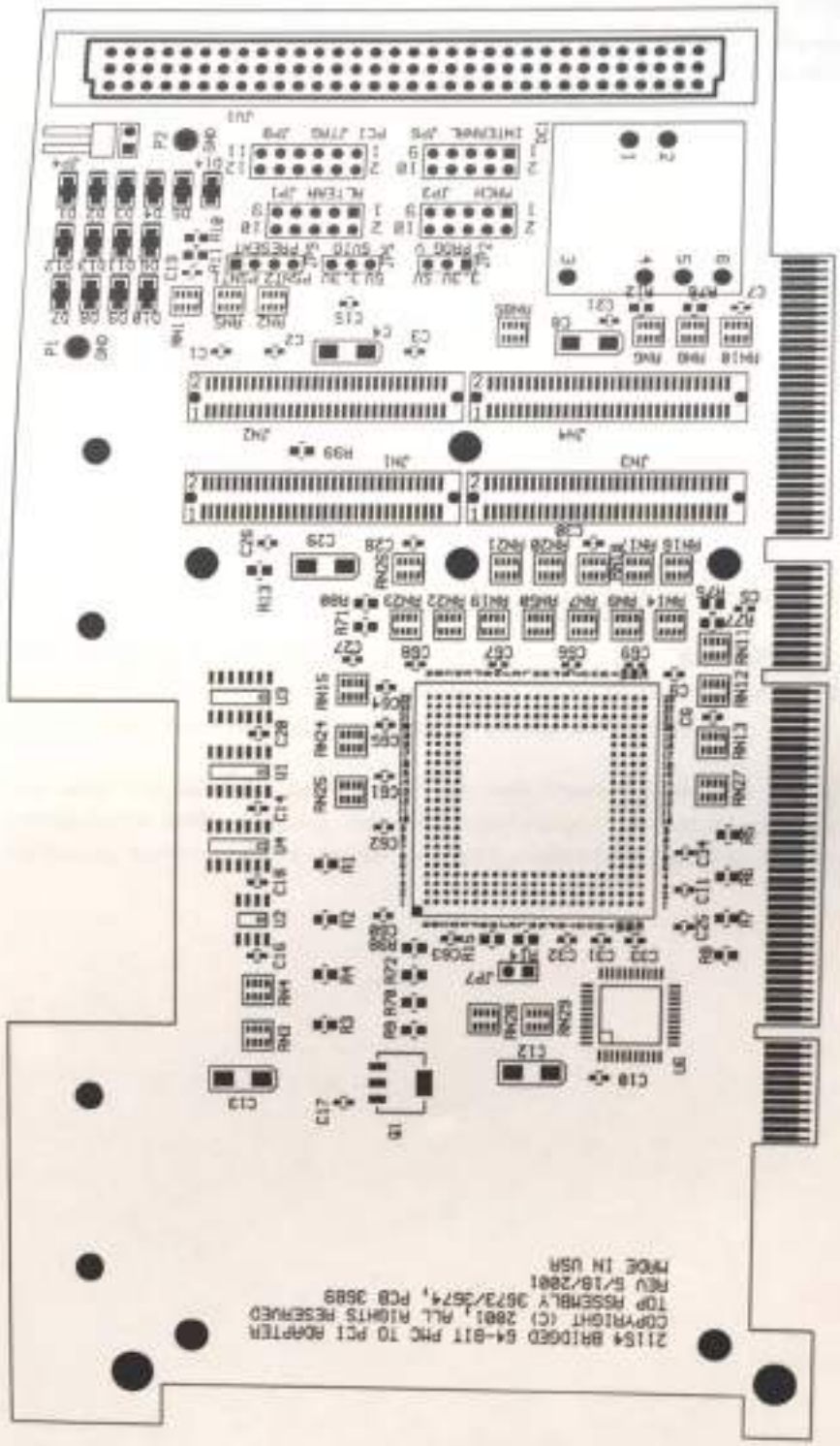
The PMC to PCI adapter requires some initialization of the 21154 PCI bridge chip for proper operation. If correctly initialized, the bridge should be "transparent" to the host operating system and the attached PMC card should appear as if it is directly connected to the host's primary PCI bus.

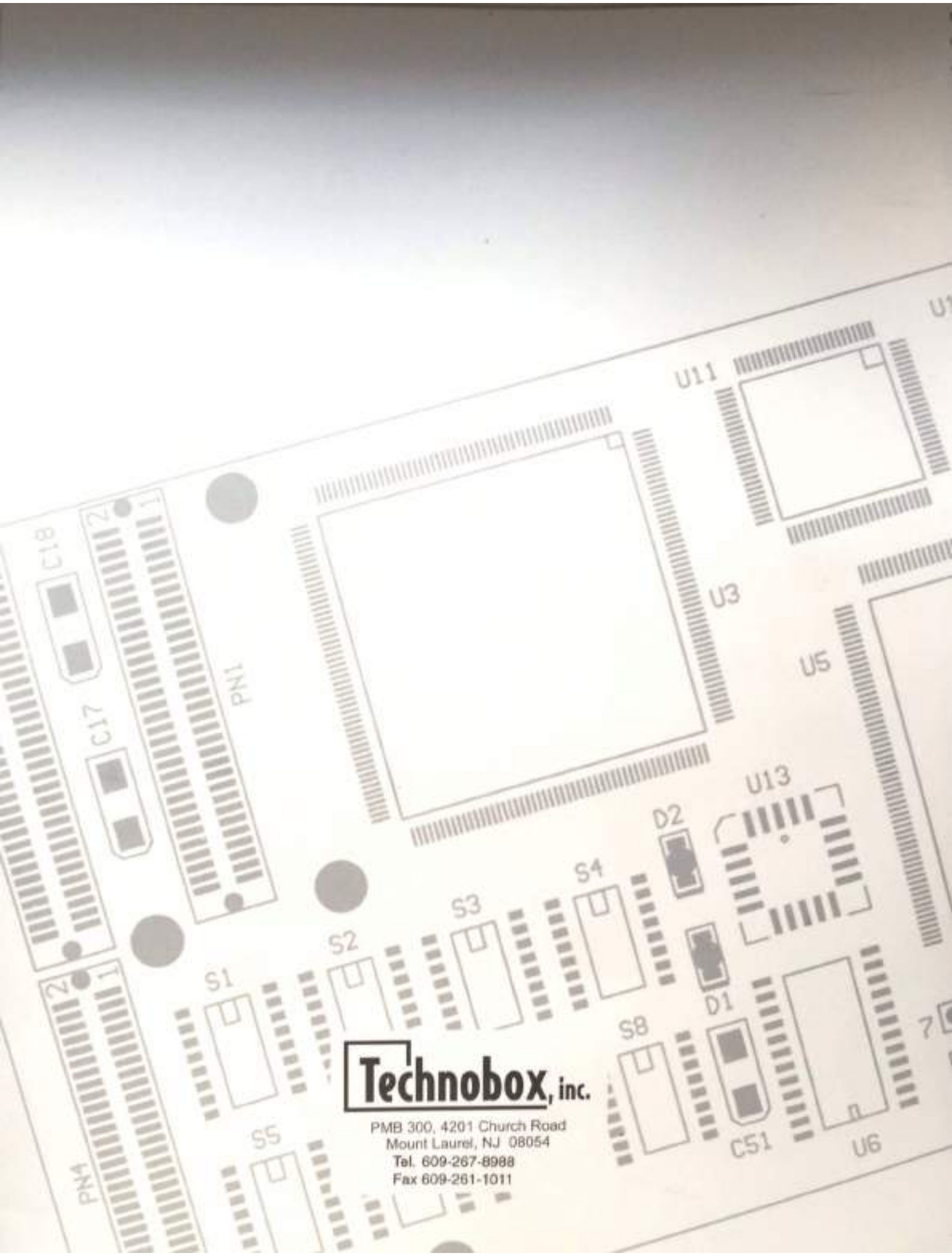
Bridge initialization is generally done by either the Motherboard BIOS and/or the Operating System. How this is accomplished depends on the user's specific hardware and firmware being employed.

The 21154 bridge chip is a fairly common device known to many operating environments, and therefore Technobox does not ship any software "drivers" for the 21154 chip. However, the user is cautioned that not all operating environments might (correctly) support the 21154 bridge chip. Please consult your hardware supplier for further details and contact Technobox for our experience with known operating environments.

The Technobox PMC to PCI adapter is tested with a 64-bit PMC SCSI card installed in a 64-bit, 66MHz, 3.3V PCI slot. It is also tested for operation in a 32-bit, 33MHz 5V slot. The specific motherboard used for this testing is an Intel STL2 populated with 700 MHz Celeron processors. This particular motherboard uses a Phoenix BIOS. Please see www.intel.com and search for "STL2" for more information.

APPENDIX A – Printed Circuit Board





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21154 BRIDGED 64-BIT PMC TO PCI ADAPTER
COPYRIGHT (C) 2001, ALL RIGHTS RESERVED
TOP ASSEMBLY 3673/3674, PCB 3689
REV 5/18/2001
MADE IN USA


MADE IN
USA
REV
070201

PMC

PCI Mezzanine Cards

Technobox, inc.

64-bit/66MHz PMC to PCI Adapter

with Intel 21154 Bridge

For Delivery Systems

Product Manual

Revision 1 – 12/15/01

Technobox, inc.

PMB 300, 4201 Church Road

Mt. Laurel, NJ 08054

(856)-778-5512

TABLE OF CONTENTS

Introduction

Block Diagram

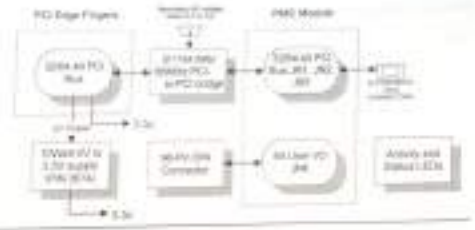

Figure 1 - Block Diagram

This 64-bit PMC-to-PCI Adapter with PCI-to-PCI bridge permits delivery of PMC-derived applications in a standard PCI environment.

This product features a 21154 PCI-to-PCI bridge chip to ensure PCI bus signal integrity even with multiple adapters plugged into a single PCI bus segment. The 21154 bridge will operate either at 33 MHz or 66 MHz PCI bus clock on either the primary or secondary side of the bridge. Dissimilar clock frequencies of 66 MHz primary side and 33 MHz secondary side works, but the 21154 does not support 33MHz on the primary side with 66 MHz on the secondary side. Any mix of 32 bit and 64 bit on the primary/secondary side is accommodated.

A 3.3V switching DC-to-DC converter is provided as a population option (order P/N 3674) on the board converts the 5V power from the PCI edge finger to 3.3V to the PMC. This allows operation in motherboards which do not support 3.3V power. The maximum current from the regulator is 3 Amps at 3.3 Volts. The other population option, P/N 3673, does not provide the DC-to-DC converter but relies 3.3V power directly from the PCI edge fingers.

Several LEDs visible from the edge of the board monitor power (PWR, 5WD, +12V, -12V, 5V, 3.3V) and key PCI bus signals (INTA, BUSMODE1, RESET#). Two LEDs sense the VIO (V, 3.3V) and key PCI bus signals (INTA, BUSMODE1, RESET#). Two LEDs sense the VIO signal voltage to indicate if the slot uses 3.3V (VIO = 3.3V) or 5V (VIO = 5V). PCI bus signaling. These two LEDs - P(VIO) and S(VIO) - indicate voltage for the primary side and secondary side PCI bus, respectively.

An optional fan assembly (P/N 3675) is available that fits over two PMC-to-PCI adapter boards and provides substantial forced-air cooling of high-power PMC modules.

The SUSMODE[4:3] inputs to the PMC is set to 00, indicating use of the PCI slot for the PMC connectors.

The user may select either 3.3V or 5V secondary PCI bus signaling levels using a jumper on the PMC to PCI adapter board. The 3.3V / 5V signaling level for the primary PCI bus is established by the "VIO" power rail on the PCI bus edge finger.

The JTAG signals going to the PMC are brought out to 10-pin headers to allow users to program their PLD and FPGA logic on the PMC card. One header is configured for ALTERA use, the other for MACH PLD use.

The 4 mil C rows of a 96-pin DIN connector, located toward the rear of the board, connect with the 64-pin user I/O connector (J6/P6) on the mezzanine card. This connection is specified by IEEE 1386 for the P2 connector on VMEbus boards and permits internal connection of rear I/O, should the PMC board support rear I/O connectivity.

A high quality 2.5 mm thick machined aluminum panel, with a 0.5 mm chamfered edge, is provided on the PCI board bracket. This ensures the mechanics of a PMC installed on a VMEbus board or other host environments and allows the PMC board to be freely positioned on the board.

Environmental

This Technobox product is a **commercial-grade** component. Accordingly, specifications are as follows:

Temperature (Operating): 0 to 55 degrees C.
Temperature (Storage): -40 to +80 degrees C.
Altitude: Not Specified or Characterized. Typical similar equipment is at 15,000 ft.
Humidity (Operating/Storage): 5% to 95% noncondensing.
Vibration: Not specified or Characterized.
MTBF: Not calculated.
Voltages Required: +12V, -12V, +5V, +3.3V (P/N 3673 only). Tol. +/-5%.
Power Required: TBD.

Part Numbers

The part numbers associated with the product are:

P/N 3673: PMC to PCI adapter – No 3.3V DC to DC converter (PMC 3.3V Power comes from PCI edge fingers)

P/N 3674: PMC to PCI adapter – With 3.3V DC to DC converter (PMC 3.3V Power comes from converter – not from PCI edge fingers)

P/N 3675: Fan assembly. Each 3675 supports **two** PMC to PCI adapters.

Revisions

Rev 0 – 6/21/00 – Initial release.

Rev 1 – 10/15/01 – added Fan Assembly installation photos and some misc.

References

This manual assumes the reader has some fundamental understanding of PCI and PMC operation as can be acquired from the following reference materials:

1. IEEE 1386 specification – Defines "Common Mezzanine Card (CMC)" mechanicals and some electrical specifications. Available from www.ieee.org.
2. IEEE 1386.1 specification – Defines PCI bus signal connection to the PMC connectors. Available from www.ieee.org.
3. Intel 21154 PCI to PCI bus bridge datasheet and related documents. Consult these if you require a better understanding of the PCI bus bridge chip used on this board. See www.intel.com.
4. PCI specification – The common industry standard PCI bus Specification is available for purchase at www.pcisig.org.

Installation

General

To install a PMC card on the PMC to PCI Adapter, seat the PMC into position on the adapter as would normally be done to install a PMC card in a VMEbus host processor application.

The PCI bracket on the adapter has been modified using a machined aluminum panel that is dimensioned to the IEEE 1386 specification. Also, the PMC has been positioned on the PMC to PCI adapter such that the PMC bezel is nominally flush with the rear surface of the PCI bracket.

The PMC bezel opening on the PCI bracket is centered with respect to the rear opening in a standard PC cabinet. This provides optimal space for the double-connector area on a PMC to protrude through the rear of a PC. However, as a result, the user will notice a slight elevation of the PMC toward the bezel, which is correct. The bezel provides metric m2.5 tapped holes to secure the PMC to the host. While these holes are flush against the host processor card, in the case of the PMC to PCI adapter, they will be approximately 1.5 mm above the corresponding holes in the PMC to PCI adapter.

It is possible to secure the PMC at the rear using PMC-supplied standoffs with m2.5 machine screws.

NOTE:

Because of the elevation of the PMC toward the front, it is not recommended that the bezel be secured via m2.5 screws as would typically be done in a PMC application. However, should the user need to secure the bezel, Technobox recommends the use of one or more flat washers between the adapter and the PMC bezel.

The opening in the PCI bracket, which accepts the PMC bezel, has been nominally machined to the IEEE 1386 specification and complies within the tolerances (0.15mm) indicated therein. However, certain PMC bezels on the market appear to be a tight fit. In these cases, it is suggested that the conductive elastomeric EMI gasket be removed to ease the installation of the PMC in the PMC to PCI Adapter.

PMC Signal Level Keying

The factory default configuration is operation of the PMC at 5V signaling levels. This is indicated by the "keying peg" located on the PMC to PCI adapter at the 5V position per the IEEE 1386 specification. Correspondingly, there is a jumper setting on the board (JP 5) which sets the Secondary PCI bus "VIO" voltage level to work at 5V.

If the PMC installed on the PMC to PCI adapter requires 3V bus signaling levels, the user should unplug and move the keying peg to the 3.3V position and also change the JP5 jumper setting for 3V signaling operation. Please see discussion of JP5 later in this manual.

PN 3675 Fan Assembly Installation

An optional P/N 3675 Fan Assembly is available to provide forced air cooling to a pair of 3672 (or 3674) PMC to PCI adapters. This scheme has been carefully designed to pull air up through the PMC card seated on the PMC to PCI adapter from the spaces around the PCI edge finger. Most motherboards will provide the PCI board sufficiently above the motherboard to provide an "intake" area for the air. The airflow is done upwards through the use of a miniature fan, which is powered from a five-pin 12-volt connector on the PMC to PCI adapter (Labeled JP4 on the silk screen legend).

A single 3675 fan assembly will handle up to two 3673/3674 PMC to PCI adapters. It is also possible to use this fan assembly on a single PMC to PCI adapter if the adjacent PCI slot is not occupied. In some cases, a short height PCI card (eg. Ethernet) might be installed in the adjacent PCI slot without interfering with the fan assembly overhang.

The 3675 fan assembly is shipped in an "assembled" fashion to keep all the parts together and also to insure the correct number and types of screws are supplied. The user must first disassemble the components, screw them down to the PMC to PCI adapter. Plug the assembly into the PCI slots, and finally attach the Fan card support plate to the rear.

A step-by-step procedure is as follows:

1. Install the PMC card(s) on the PMC to PCI adapter(s).
2. Detach the four "U" shaped channels from the fan plate as shipped from Technobox. Keep the fan attached to the fan plate.
3. Attach two "U" shaped channels to each PMC to PCI adapter as shown in the photograph. Keep the threaded PEM fasteners upward in order to later receive securing of the fan plate. Use the screws from step 1, and please make sure to install the lock-washer and flat-washer on the screw-head side of the printed circuit board(s). The flat-washer goes against the printed circuit board, while the lock-washer goes against the screw head.
4. Install the PMC to PCI adapter(s) in the target machine as shown in the photograph. Make sure the edge fingers are properly seated in the motherboard. Don't screw down the PCI bracket yet, since doing so will hamper proper alignment of the fan plate screw openings with the threaded PEM nuts.
5. Attach Fan Plate (with fan) to the seated PMC to PCI adapters. Use a total of 8 screws. Make sure to install the lock-washer and flat-washer on the screw-head side of the fan plate. The flat-washer goes against the fan plate, while the lock-washer goes against the screw head.
6. With the fan plate secured and the PMC to PCI adapter(s) properly seated in their respective PCI slot(s), screw down the PCI bracket to the target machine.
7. Connect the fan power line to JP4 of any one of the installed PMC to PCI adapters. The connector is keyed to assure proper voltage polarity. In this case, RED is +12V, and BLACK is GROUND.

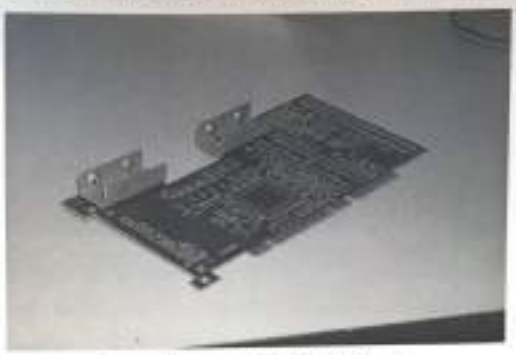

Figure 3 - U channels attached to PMC to PCI adapter

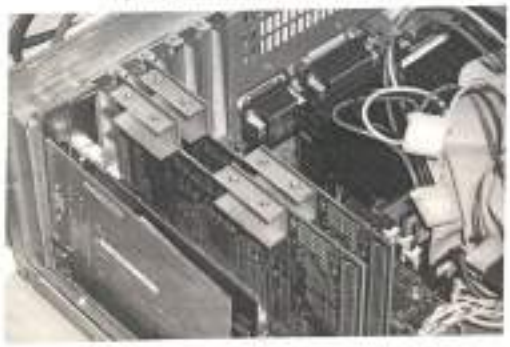

Figure 3 - Two PMC to PCI adapters ready to receive Fan Plate

Figure 4 – Two PMC to PCI adapters showing Fan Plate installed

Note that these early photos show a depopulated PMC to PCI adapter board with no PMC installed and no PCI Bracket. However, the reader should be able to interpret these photos for correct fan installation.

Operation and Configuration

PCI PRESENT Signals

The PCI specification identifies two PRESENT signals on the PCI connector that corresponds to the power dissipation of the PCI board. In concept, these signals can be monitored by an intelligent host design to identify power supply overloading situations.

The state of the PRESENT 1 and PRESENT 2 signals are controlled by two Push-on jumpers located at JP9 on the board as follows:

Signal	PCI edge finger a/n	IN	OUT	JP9 Pin #'s
PRESENT1	B9	GROUND (Default)	OPEN	1-2
PRESENT2	B31	GROUND (Default)	OPEN	3-4

Table 1 - Jumpers for PCI PRESENT 1 and PRESENT 2 (JP9)

Note that "VIN1" and "VIN2" legends on the Silk Screen on the Printed Circuit Board help identify the positions of these jumpers on JP9, as well as a "PRESENT" label next to JP9. Also, a square pad on the Printed Circuit board solder-side indicates JP9 pin number 1.

In the normal configuration as shipped from the factory, both jumpers are installed, thereby grounding both PRESENT 1 and PRESENT 2 signals.

BUSMODE Signals

The BUSMODE signals are unique to the IEEE 1386, and are not found in the PCI specification. They allow a host that supports connectivity to an IEEE 1386 board, to identify whether an IEEE or PCIBUS interface is installed. Essentially, three BUSMODE signals (bits [4..2]) are driven by the Host Processor with a code defined by the IEEE specification, and the Common Mezzanine Card (CMC) should respond with BUSMODE[1] asserted if it is supported by the requested bus mode.

The PMC to PCI adapter presents a 001 pattern on the BUSMODE[4..2] signals to the PMC card. This encoding is for PCI bus applications.

A properly designed PMC module should assert BUSMODE[1] when it sees the 001 pattern on BUSMODE[4..2]. An LED on the PMC to PCI adapter – D6 – is illuminated when BUSMODE[1] is asserted. The asserted state of BUSMODE[1] is LOW.

32-bit/64-bit bus width support – Primary PCI bus side

Operation of the PCI bus at 32-bit or 64-bit width on the Primary PCI bus side of the 21154 bridge chip is automatically selected by PCI bus protocol. This is accomplished via the PCI bus C/BE7..4] lines together with the REQ64 and GNT64 lines.

32-bit/64-bit bus width support – Secondary PCI bus side

Operation of the PCI bus at 32-bit or 64-bit width on the Primary PCI bus side of the 21154 bridge chip is automatically selected by PCI bus protocol. This is accomplished via the PCI bus C/BE7..4] lines together with the REQ64 and GNT64 lines.

The 21154 bridge chip will consecutively push/unpack words between 32-bit and 64-bit systems. Except for performance, this is totally transparent to the user.

33/66MHz clock speed support – Primary PCI bus side

Support for 33MHz or 66MHz clock speed on the Primary PCI bus side of the 21154 bridge chip is determined by the "M66EN" signal on the edge finger connector. This is located on edge finger pin B49.

PCI bus slots which only support 33 MHz will bond this signal lead to GROUND. Otherwise, it will be HIGH and there is a pull-up on the PMC to PCI adapter to assure a solid HIGH signal. The 21154 bridge chip senses the state of M66EN to determine the operating speed of the Primary PCI bus.

33/66MHz clock speed support – Secondary PCI bus side

Support for 33MHz or 66MHz clock speed on the Secondary PCI bus side of the 21154 bridge chip is determined by the "M66EN" signal on the PMC connector. This is located on jam pin/PN2 pin A7.

PMC cards plugged into the PMC to PCI adapter which only support 33 MHz will bond this signal lead to GROUND. Otherwise, it will be HIGH and there is a pull-up on the PMC to PCI adapter to assure a solid HIGH signal. The 21154 bridge chip senses the state of M66EN to determine the operating speed of the Secondary PCI bus.

3V/5V PCI Signaling Environment – Primary PCI bus side

This PMC to PCI adapter is keyed on the PCI edge fingers for "universal" operation. That is, the PMC to PCI adapter may be plugged into either a 3V signaling environment or a 5V signaling environment and operate correctly. This is accomplished through the use of the "VIO" power rail on the PCI edge fingers, which connect to the 21154 bridge chip Primary VIO signal.

There are no jumpers required to configure the **Primary** PCI bus side signaling level. Again, it's done automatically through the VIO voltage level on the PCI edge fingers as presented to the PMC to PCI adapter.

3V/5V PCI Signaling Environment – Secondary PCI bus side

The PMC to PCI adapter may be set up for PMC operation at either 3.3V or 5V signaling levels. This is accomplished by a jumper setting "JP5" on the board. Also, the voltage keying peg should be positioned according to the signaling voltage level required by the installed PMC card. The factory default configuration is 5V signaling for the PMC card.

JP5 sets the secondary side of the 21154 PCI to PCI bridge chip for 3V or 5V operation per the following table. The correct position of the keying peg is also noted in this table.

PMC operation	JP5 Pin #'s for jumper	Keying Peg
3V signaling	2-3	3V position
5V signaling	1-2 (default)	5V position (default)

Table 2 – PCI bus secondary signal levels (JP5)

Only one push-on jumper can be installed on JP5. Note that for proper operation a push-on jumper must be installed in either the 1-2 position for 5V operation, or the 2-3 position for 3V operation.

For user convenience, the silk screen legend on the board shows "5V/3V" near JP5 connector as an indication that this connector is used for configuring the Secondary PCI VIO rail. Also, "5V" and "3.3V" legends indicate the jumper position for 5V and 3V operation, respectively.

32/64bit, 3V/5V signaling, 33/66MHz valid combinations

By virtue of the 21154 bridge chip used on this board, connection between PCI bus and PMC bus having different bus widths (32-bit, 64-bit), clock frequencies (33MHz, 66MHz) and PCI bus signaling levels (3V, 5V) is possible. Due to restrictions imposed by the 21154 chip, not all combinations are valid, however. For example, operation of a 33MHz PMC card in a 66MHz PCI slot is possible, but not the other way around.

A table showing valid combinations of bus width, signaling, and clock speed follows. The table headers consist of 3 numbers – ***X Y Z*** – representing the bus width, clock speed, and signaling levels, respectively.

		PRIMARY SIDE PCI BUS (PCI edge fingers)							
	X Y Z	32 33 3	32 33 5	32 66 5	32 66 3	64 33 3	64 33 5	64 66 5	64 66 3
Secondary Side PCI Bus (PMC CARD)	32 33 3	OK	OK	OK	Invalid	OK	OK	OK	Invalid
	32 33 5	OK	OK	OK	Invalid	OK	OK	OK	Invalid
	32 66 5	Invalid	Invalid	OK	Invalid	Invalid	Invalid	OK	Invalid
	32 66 3	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
	64 33 3	OK	OK	OK	Invalid	OK	OK	OK	Invalid
	64 33 5	OK	OK	OK	Invalid	OK	OK	OK	Invalid
	64 66 5	Invalid	Invalid	OK	Invalid	Invalid	Invalid	OK	Invalid
	64 66 3	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid

Table 3 – Valid combinations of clock,signaling,bus width

Operation at 66 MHz in a 5V signaling environment is not recommended, hence the "invalid" entries for this combination in the table.

Combinations where Primary PCI bus operate at 33MHz and secondary PCI bus operate at 66 MHz is not supported by the 21154 bridge chip.

Power Supply Environment

PCI/PMC defines a variety of supply voltages available to a card:

- 3.3vDC to supply 3.3V logic
- 5.0vDC to supply 5V logic
- +12VDC to supply RS232, Analog, etc.
- -12VDC to supply RS232, Analog, etc.

According to the PCI specification, 3.0VDC, +12VDC, and -12VDC supplies are mandatory. However, the 3.3VDC supply is optional, and the PCI specification suggests that motherboard vendors have some way of enhancing their systems with an upgrade kit.

In our experience, we have found the majority of recently manufactured Pentium motherboards to supply 3.3V power to the PCI slots without any special hardware. However, we have also come across some older motherboards that don't supply 3.3V power to the PCI slots.

Customers who are using motherboards that supply 3.3V to the PCI bus edge fingers should be using Technobox P/N 3673. In the unlikely case where your motherboard does not support 3.3V power to the PCI slots, the Technobox P/N 3674 provides a 10watt on-board DC-to-DC converter located at reference designator "DC1" on the board. This is a 1" square package that converts 5VDC from the PCI edge fingers to 3.3V going to the logic on the PMC by PCI adapter as well as the PMC site.

Indicator LEDs

Fourteen GREEN indicator LEDs located at the top edge of the board provide a quick indication of the activity and state of the PCI bus and power supplies. The function of these LEDs are noted on the silk-screen legend of the board, on the side opposite to the LEDs. These LEDs are also summarized below:

/INTA – On when "/INTA" is LOW (asserted) on the PCI bus.

/INTB – On when "/INTB" is LOW (asserted) on the PCI bus.

/INTC – On when "/INTC" is LOW (asserted) on the PCI bus.

/INTD – On when "/INTD" is LOW (asserted) on the PCI bus.

3V3VIO – On when the VIO power rail on the Primary PCI bus is greater than approximately 4.5 volts, indicating use of a 5V signaling PCI bus. Otherwise, off (i.e., 3.3V PCI signaling is in use).

3V3VS – On when the VIO power rail on the Secondary PCI bus is greater than approximately 4.5 volts, indicating use of a 5V signaling PCI bus. Otherwise, off (i.e., 3.3V PCI signaling is in use).

REQ – On when the PMC board is asserting 32-bit Bus Request to the PCI bus. Should flicker during bus master operation.

BUSMODE – On when the PMC card is driving BUSMODE[1] LOW. If PMC supports BUSMODE, this LED should be ON.

-12V – On when -12V power rail is supplied with voltage. Should always be ON.

+12V – On when +12V power rail is supplied with voltage. Should always be ON.

+5V – On when 5V power rail is supplied with voltage. Should always be ON.

+3.3V – On when 3.3V power rail is supplied with voltage. Should always be ON.

PVIO – On when Primary PCI bus VIO power rail is supplied with voltage. Should always be ON.

5VIO – On-board Primary PCI bus VIO power rail is supplied with voltage. Should always be ON.

JTAG Connector – JP8 (PCI bus to 21154 chip)

JP8, located next to the DIN connector on the right side of the board, is used to connect the PCI bus "JTAG" signals to the Intel 21154 bridge chip. Normally, the jumpers are **not** installed, as a JTAG connection to the 21154 chip is **not** made.

The pin numbering for JP8 connector is indicated on the silk screen. The signal definitions are summarized here:

Pin #1 – PCI TDI	Pin #2 – 21154 TDI
Pin #3 – PCI TDO	Pin #4 – 21154 TDO
Pin #5 – PCI TCK	Pin #6 – 21154 TCK
Pin #7 – PCI TMS	Pin #8 – 21154 TMS
Pin #9 – PCI TRST	Pin #10 – 21154 TRST
Pin #11 – Ground	Pin #12 – Ground

To support the convention that TDO is tied to TDI for PCI bus cards that don't support or need JTAG, JP8 is populated with a jumper between pins 1 and 2. There should not be any other jumpers applied to JP8.

The JTAG connections to the PMC connectors are done through "ALTERA" and "MACH" JTAG headers JP1 and JP2 on the PMC to PCI adapter. These are discussed in subsequent sections.

JTAG Connector – JP1 (ALTERA)

The PMC "JTAG" signals – TDI, TDO, TRST, TMS, and TCK – are connected to 10-pin headers JP1 and JP2 on the PMC to PCI adapter. These are intended to be used for programming either ALTERA FPGA or LATTICE MACH devices on the user's PMC board.

Specifically, JP1 is used to connect a personal computer Parallel Port using ALTERA's "ByteBlasterMV" cable. The pinout of JP1 is as follows:

Signal	PMC connection	JP1 connection
TCK	PN1/JN1 – 1	1
GND	N/A	2
TDO	PN1/JN1 – 4	3
3.3V or 5V (*)	N/A	4
TMS	PN1/JN1 – 3	5
3.3V or 5V (*)	N/A	6
N/C	N/A	7
N/C	N/A	8
TDI	PN1/JN1 – 5	9
GND	N/A	10

Table 4- ALTERA JTAG header (JP1)

(*) – This is the power to the ALTERA cable. It is either 3.3V or 5V depending on JP2 jumper selection.

JP1 is also identified as "ALTERA" on the PMC to PCI adapter printed circuit board silk screened legend.

N/C – no connection inside

N/A – Not applicable

JTAG Connector – JP2 (LATTICE)

For those PMC implementations using LATTICE devices (eg. MACH banks), and needing JTAG programming through the PMC's JTAG signals, the PMC to PCI adapter provides a header – JP2 – for connection to LATTICE's ispPRO programming cable.

The pinout of JP2 is as follows:

Signal	PMC connection	JP1 connection
TCK	PN1/JN1 – 1	1
GND	N/A	2
TMS	PN1/JN1 – 3	3
GND	N/A	4
TDI	PN1/JN1 – 5	5
3.3V or 5V (*)	N/A	6
TDO	PN1/JN1 – 4	7
GND	N/A	8
TRST	PN1/JN1 – 2	9
N/C	N/A	10

Table 5- LATTICE JTAG header (JP2)

(*) – This is the power to the MACH cable. It is either 3.3V or 5V depending on JP2 jumper selection.

JP2 is also identified as "MACH" on the PMC to PCI adapter printed circuit board silk screened legend.

N/C – No connection inside

N/A – Not applicable

JTAG voltage level select jumper – JP2 (for ALTERA/MACH)

The LATTICE and ALTERA programming cables require a power supply from the target in order to power the logic in the cable. This power supplied is either 3.3V or 5V depending on the technology of the devices you are attempting to program.

The PMC to PCI adapter provides a jumper setting to select between 3.3V or 5V power to the JTAG programming headers. This jumper header is labeled "JP2" on the silk screen legend.

The 3.3V and 5V positions are established according to the following table:

JTAG cable operation	JP2 Pin #'s for jumper
3V	2-3
5V	1-2 (default)

Table 6 - JTAG voltage level select (JP2)

For user convenience, the silk screen legend on the board shows "PROG" over JP5 connector as an indication that this connector is used for configuring the JTAG cable power. Also, "5V" and "3.3V" legends indicate the jumper position for 5V and 3V operation, respectively.

JTAG Connector – JP6 (Internal Use Only)

Customers should NOT use the 10-pin connector identified as "JP6" and "INTERNAL" on the silk screen legend. This connector is used during the manufacture of the PMC to PCI adapter to effect programming of the PLD located on the board.

64-pin DIN Connectors

The 96-pin DIN connector is located at the right edge of the PMC to PCI Adapter. Its purpose is to match the connection of the USER I/O connector (J4/J5/J6) on the PMC module to the "A" and "C" rows of the P2 connector on a VMEbus board. This connection is fully defined in the IEEE 1386 specification and it adheres to the following numbering strategy:

PMC I/O Pin Number	VMEbus P2 Connector Pin Number
1	c1
2	a1
3	c2
4	a2
(Continue similarly)	
63	c32
64	a32

The c1 (PMC I/O 1) connection is located near the upper edge of the PMC-to-PCI adapter board, whereas the c32 connection (PMC I/O 64) is located closest to the PCI connector.

The markings stamped on the DIN connector may be different than this because of the reverse nature of the user I/O connector on VME backplanes. Please disregard any A and C row markings that may be stamped on the connector.

The user should fully understand the relationship between the DIN contacts and the J4/J5 connections before using the DIN connector. An ohmmeter is a helpful tool to check continuity between these connectors and understand the theory of operation.

Software

The PMC to PCI adapter requires some initialization of the 21154 PCI bridge chip for proper operation. If correctly initialized, the bridge should be "transparent" to the host operating system and the attached PMC card should appear as if it is directly connected to the host's primary PCI bus.

Bridge initialization is generally done by either the Motherboard BIOS and/or the Operating System. How this is accomplished depends on the user's specific hardware and firmware being employed.

The 21154 bridge chip is a fairly common device known to many operating environments, and therefore Technobox does not ship any software "drivers" for the 21154 chip. However, the user is cautioned that not all operating environments might (correctly) support the 21154 bridge chip. Please consult your hardware supplier for further details and contact Technobox for our experience with known operating environments.

The Technobox PMC to PCI adapter is tested with a 64-bit PMC SCSI card installed in a 64-bit, 66MHz, 3.3V PCI slot. It is also tested for operation in a 32-bit, 33MHz 5V slot. The specific motherboard used for this testing is an Intel STL2 populated with 700 MHz Celeron processors. This particular motherboard uses a Phoenix BIOS. Please see www.intel.com and search for "STL2" for more information.

APPENDIX A – Printed Circuit Board