Motorola 68000 CPU Opcodes

Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Ext. word (15–8)	Ext. word (7–0)	Ext. word 2
ORI to CCR	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0 0 0 0 0 0 0 0	CCR	
ORI to SR	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	SR		
ORI	0	0	0	0	0	0	0	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
ANDI to CCR	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0 0 0 0 0 0 0 0	CCR	
ANDI to SR	0	0	0	0	0	0	1	0	0	1	1	1	1	1	0	0	SR		
ANDI	0	0	0	0	0	0	1	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
SUBI	0	0	0	0	0	1	0	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
ADDI	0	0	0	0	0	1	1	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
EORI to CCR	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	0	0 0 0 0 0 0 0 0	CCR	
EORI to SR	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	SR		
EORI	0	0	0	0	1	0	1	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
CMPI	0	0	0	0	1	1	0	0	S		M			Xn			16 bit Data	8 bit Data	32 bit Data
BTST	0	0	0	0	1	0	0	0	0	0	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BCHG	0	0	0	0	1	0	0	0	0	1	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BCLR	0	0	0	0	1	0	0	0	1	0	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BSET	0	0	0	0	1	0	0	0	1	1	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BTST	0	0	0	0	Dn			1	0	0	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BCHG	0	0	0	0	Dn			1	0	1	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BCLR	0	0	0	0	Dn			1	1	0	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
BSET	0	0	0	0	Dn			1	1	1	M			Xn			0 0 0 0 0 0 0 0	Bit Index	
MOVEP	0	0	0	0	Dn			1	D	S	0	0	1	An			Displacement		
MOVEA	0	0	S		An			0	0	1	M			Xn					
MOVE	0	0	S		Xn			M			M			Xn					
MOVE from SR	0	1	0	0	0	0	0	0	1	1	M			Xn					
MOVE to CCR	0	1	0	0	0	1	0	0	1	1	M			Xn					
MOVE to SR	0	1	0	0	0	1	1	0	1	1	M			Xn					
NEGX	0	1	0	0	0	0	0	0	S		M			Xn					
CLR	0	1	0	0	0	0	1	0	S		M			Xn					
NEG	0	1	0	0	0	1	0	0	S		M			Xn					
NOT	0	1	0	0	0	1	1	0	S		M			Xn					
EXT	0	1	0	0	1	0	0	0	1	S	0	0	0	Dn					
NBCD	0	1	0	0	1	0	0	0	0	0	M			Xn					
SWAP	0	1	0	0	1	0	0	0	0	1	0	0	0	Dn					
PEA	0	1	0	0	1	0	0	0	0	1	M			Xn					
ILLEGAL	0	1	0	0	1	0	1	0	1	1	1	1	1	1	0	0			
TAS	0	1	0	0	1	0	1	0	1	1	M			Xn					
TST	0	1	0	0	1	0	1	0	S		M			Xn					
TRAP	0	1	0	0	1	1	1	0	0	1	0	0	Vector						
LINK	0	1	0	0	1	1	1	0	0	1	0	1	0	An			Displacement		
UNLK	0	1	0	0	1	1	1	0	0	1	0	1	1	An					
MOVE USP	0	1	0	0	1	1	1	0	0	1	1	0	D	An					
RESET	0	1	0	0	1	1	1	0	0	1	1	1	0	0	0	0			
NOP	0	1	0	0	1	1	1	0	0	1	1	1	0	0	0	1			
STOP	0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	0	Immediate		

Addressing mode	Format	M	Xn
Data register	Dn	0 0 0	reg
Address register	An	0 0 1	reg
Address	(An)	0 1 0	reg
Address with Postincrement	(An)+	0 1 1	reg
Address with Predecrement	-(An)	1 0 0	reg
Address with Displacement	(d_{16}, An)	1 0 1	reg
Address with Index	(d_8, An, Xn)	1 1 0	reg
ProgrAn Counter with Displacement	(d_{16}, PC)	1 1 1	0 1 0
ProgrAn Counter with Index	(d_8, PC, Xn)	1 1 1	0 1 1
Absolute Short	(xxx).W	1 1 1	0 0 0
Absolute Long	(xxx).L	1 1 1	0 0 0
Immediate	#imm	1 1 1	1 0 0

Operation Size	Suffix	S	S
Byte	.b	0 0	/
Word	.w	0 1	0
Long	.l	1 0	1

Condition	Mnemonic	Cond
True	T	0 0 0 0
False	F	0 0 0 1
Higher	HI	0 0 1 0
Lower or SAne	LS	0 0 1 1
Carry Clear	CC	0 1 0 0
Carry Set	CS	0 1 0 1
Not Equal	NE	0 1 1 0
Equal	EQ	0 1 1 1
Overflow Clear	VC	1 0 0 0
Overflow Set	VS	1 0 0 1
Plus	PL	1 0 1 0
Minus	MI	1 0 1 1
Greater or Equal	GE	1 1 0 0
Less Than	LT	1 1 0 1
Greater Than	GT	1 1 1 0
Less or Equal	LE	1 1 1 1

by GoldenCrystal

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RTE	0 1 0 0	1 1 1 0 0 1 1 1 0 0 1 1														
RTS	0 1 0 0	1 1 1 0 0 1 1 1 0 1 0 1														
TRAPV	0 1 0 0	1 1 1 0 0 1 1 1 0 1 1 0														
RTR	0 1 0 0	1 1 1 0 0 1 1 1 0 1 1 1														
JSR	0 1 0 0	1 1 1	0 1 0	M	Xn											
JMP	0 1 0 0	1 1 1	0 1 1	M	Xn											
MOVEM	0 1 0 0	1	D	0	0 1	S	M	Xn	Register List Mask							
LEA	0 1 0 0	An		1 1 1	M	Xn										
CHK	0 1 0 0	Dn		1 1 0	M	Xn										
ADDQ	0 1 0 1	Data		0	S	M	Xn									
SUBQ	0 1 0 1	Data		1	S	M	Xn									
Scc	0 1 0 1	Condition		1 1	M	Xn										
DBcc	0 1 0 1	Condition		1 1	0 0 1	Dn	16 bit Displacement									
BRA	0 1 1 0	0 0 0 0	Displacement	16 bit Displacement												
BSR	0 1 1 0	0 0 0 1	Displacement	16 bit Displacement												
Bcc	0 1 1 0	Condition		Displacement	16 bit Displacement											
MOVEQ	0 1 1 1	Dn	0	Data												
DIVU	1 0 0 0	Dn		0 1 1	M	Xn										
DIVS	1 0 0 0	Dn		1 1 1	M	Xn										
SBCD	1 0 0 0	Xn		1 0 0 0 0	M	Xn										
OR	1 0 0 0	Dn	D	S	M	Xn										
SUB	1 0 0 1	Dn	D	S	M	Xn										
SUBX	1 0 0 1	Xn		1	S	0 0	M	Xn								
SUBA	1 0 0 1	An		S	1 1	M	Xn									
EOR	1 0 1 1	Dn		1	S	M	Xn									
CMPM	1 0 1 1	An		1	S	0 0 1	An									
CMP	1 0 1 1	Dn		0	S	M	Xn									
CMPA	1 0 1 1	An		S	1 1	M	Xn									
MULU	1 1 0 0	Dn		0	1 1	M	Xn									
MULS	1 1 0 0	Dn		1	1 1	M	Xn									
ABCD	1 1 0 0	Xn		1 0 0 0 0	M	Xn										
EXG	1 1 0 0	Xn		1	M	0 0	M	Xn								
AND	1 1 0 0	Dn	D	S	M	Xn										
ADD	1 1 0 1	Dn	D	S	M	Xn										
ADDX	1 1 0 1	Xn		1	S	0 0	M	Xn								
ADDA	1 1 0 1	An		S	1 1	M	Xn									
ASL/ASR	1 1 1 0	0 0 0	D	1 1	M	Xn										
LSL/LSR	1 1 1 0	0 0 1	D	1 1	M	Xn										
ROXL/ROXR	1 1 1 0	0 1 0	D	1 1	M	Xn										
ROL/ROR	1 1 1 0	0 1 0	D	1 1	M	Xn										
ASL/ASR	1 1 1 0	Dn/Data	D	S	M	0 0	Dn									
LSL/LSR	1 1 1 0	Dn/Data	D	S	M	0 1	Dn									
ROXL/ROXR	1 1 1 0	Dn/Data	D	S	M	1 0	Dn									
ROL/ROR	1 1 1 0	Dn/Data	D	S	M	1 1	Dn									

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Long	.l	1	0

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Greater Than	GT	1 1 1 0
Less or Equal	LE	1 1 1 1